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An Efficient Implementation of Carry Select Adder with Low Power and Area Efficient Characteristics

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Abstract: The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum . However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input , then the final sum and carry are selected by the multiplexers (mux). The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA to achieve high speed and low power consumption.

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Keywords:Low Power VLSI, Carry select, RCA, BEC, VLSI

I. INTRODUCTION

The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem. The basic idea of the proposed work is using n-bit Binary to Excess-1 Converters (BEC) to improve the speed of addition. This logic can be implemented with Carry Select Adder to Achieve Low Power and Area Efficiency. The proposed 32-bit Carry Select Adder compared with the Carry Skip Adder (CSKA) and Regular 32-bit Carry Select Adder. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin = 0 and Cin = 1, then the final sum and carry are selected by the multiplexers (mux). The entire work performed by usage of Binary to Excess-1 Converter (BEC) instead of RCA with Cin = 1 in the regular CSLA to achieve lower power consumption The main advantage of this BEC logic comes from the lesser number of logic gates than the n- bit Ripple Carry Adder (RCA). A structure of 4-bit BEC and the truth table is shown in Fig.1 and Table 1 respectively

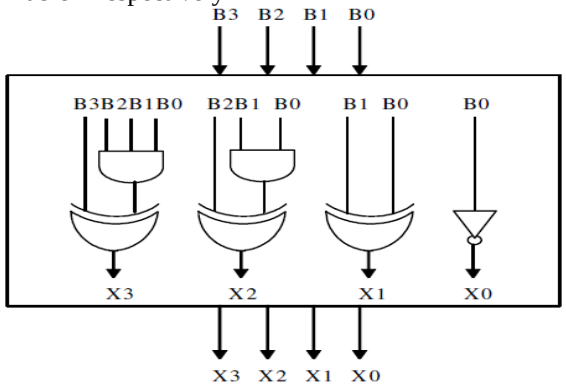

Fig.1. A 4-bit Binary to Excess-1 Converter (BEC)

Table.1 : Functional Table of 4-Bit BEC

B [3 : 0]	X [3 : 0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

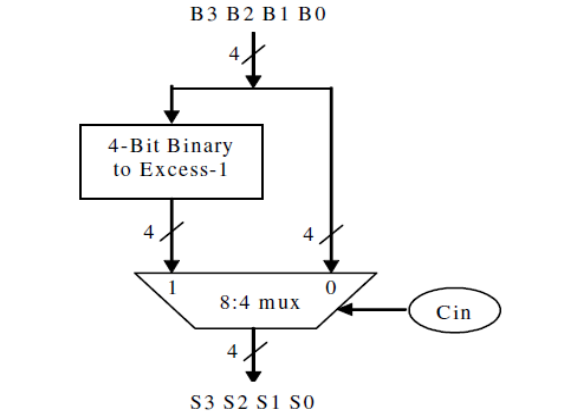

Fig.2. 4-b BEC with 8:4 mux

The goal of fast addition is achieved using BEC together with a multiplexer (mux) is described in Fig.1.2, one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the Mux is the BEC output. This produces the two possible partial product results in parallel and the Muxes are used to select either BEC output or the direct inputs according to the control signal Cin.

II. EXISTING SYSTEM

A carry-skip adder consists of a simple ripple carry-adder with a special speed up carry chain called a skip chain. Carry skip adder is a fast adder compared to ripple carry adder when addition of large number of bits take place; carry skip adder has $O(\sqrt{n})$ delay provides a

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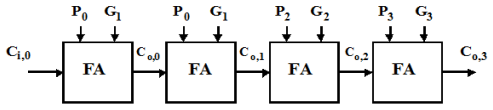
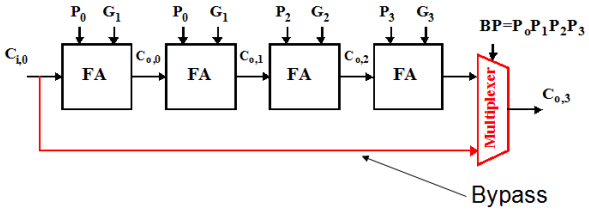
good compromise in terms of delay, along with a simple and regular layout This chain defines the distribution of ripple carry blocks, which compose the skip adder. A carry-skip adder is designed to speed up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder. Actually the ripple carry adder is faster for small values of N. However the industrial demands these days, which most desktop computers use word lengths of 32 bits like multimedia processors, makes the carry skip structure more interesting. The basic structre of Carry Skip Adder is shown in Fig.3.



(a)Carry Propagation



(b) Adding By Pass

Fig.3. Carry skip adder structure – basic concept

The crossover point between the ripple-carry adder and the carry skip adder is dependent on technology considerations and is normally situated 4 to 8 bits. The carry-skip circuitry consists of two logic gates. The AND gate accepts the carry-in bit and compares it to the group propagate signal using the individual propagate values. A carry-skip adder reduces the carry-propagation time by skipping over groups of consecutive adder stages. The carry-skip adder is usually comparable in speed to the carry look-ahead technique, but it requires less chip area and consumes less power.

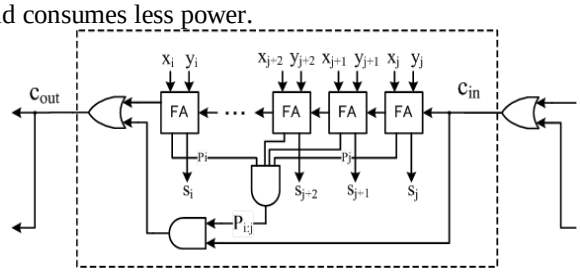


Fig.4. Carry Skip Adder

In the carry-skip adder, any adder stage can be skipped for which Pm = xm exor ym = 1, where Pm indicates the m th carry propagate. The adder structure is divided into blocks of consecutive stages with a simple ripple-carry scheme. Every block also generates a block-carry-propagate signal that equals 1 if all stages internal to the block satisfy Pm = 1. This signal can be used to allow an incoming carry to skip all the stages within the block and generate a block-carry-out. Fig.4 shows an example block consisting of k bit positions j, j+1, ..., j+k-1.

Carry Skip Mechanics

Boolean Equations

Carry Propagate: $P_i = A_i \square B_i$

Sum: $S_i = P_i \square C_i$

Carry Out: $C_{i+1} = A_i B_i + P_i C_i$

If $A_i = B_i$ then $P_i = 0$, making the carry out, C_{i+1}, depend only on A_i and B_i $\square$ $C_{i+1} = A_i B_i$

$C_{i+1} = 0$ if $A_i = B_i = 0$

$C_{i+1} = 1$ if $A_i = B_i = 1$

Alternatively if $A_i \square B_i$ then $P_i = 1$ $\square$ $C_{i+1} = C_i$. And the example is shown below

Two Random Bit Strings:

A	10100	01011	10100	01011
B	01101	10100	01010	01100
	Block 3	block 2	block 1	block 0

Compare the two binary strings inside each block. If all the bits inside are unequal, block 2, then the carry in from block 1 is propagated to block 3 Carry-ins from block 2 receive the carry in from block 1 If there exists a pair of bits that is equal carry skip mechanism fails.

Carry Skip Adder Drawbacks

The carry skip adder is unfortunately still linear in the number of bits N. Despite of its linear feature, the slope of the delay function increases in a more gradual fashion than the ripple-carry adder. Actually the ripple carry adder is faster for small values of N. However the industrial demands these days, which most desktop computers use word lengths of 32 bits, even longer for severs and multimedia processors, makes the carry skip structure more interesting. The crossover point between the ripple-carry adder and the carry skip adder is dependent on technology considerations and is normally situated 4 to 8 bits.

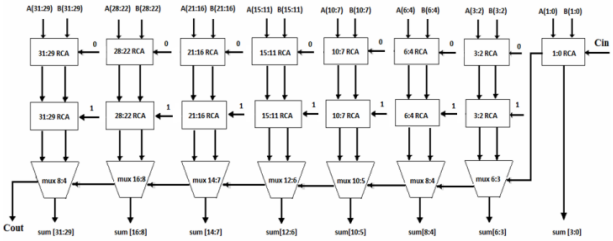
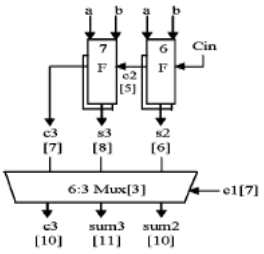
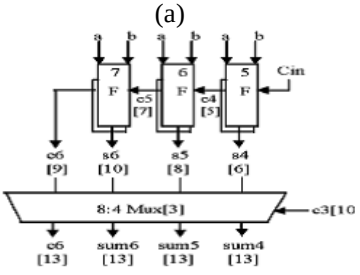


Fig. 5. 32 bit regular carry select adder

The structure of the 32-bit Carry Select Adder is shown in Fig.5. It has five groups of different size Ripple Carry Adders.



(a)



(b)

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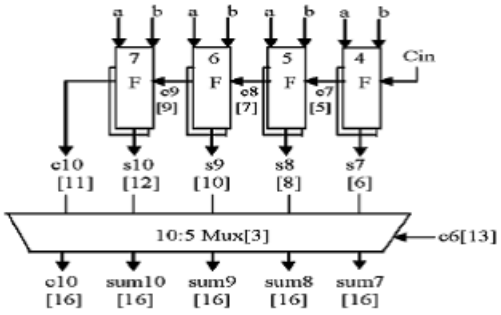
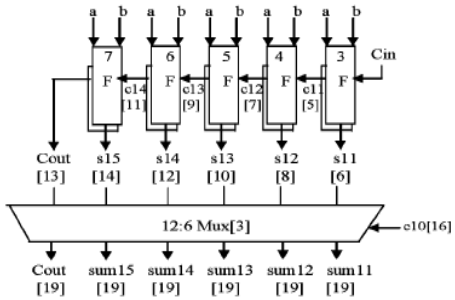


(c)

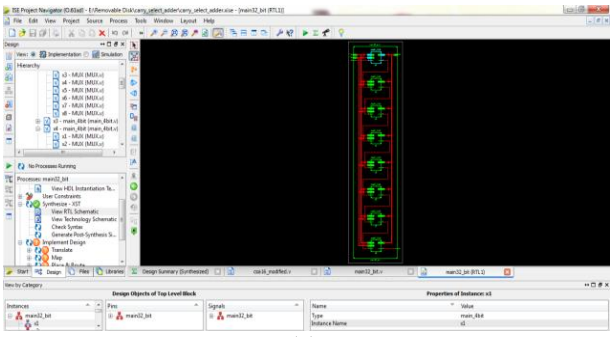


(d)

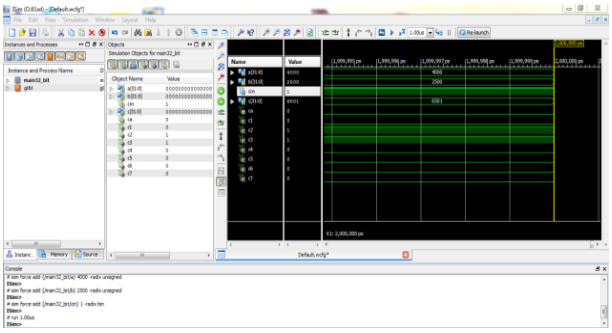
Fig.6. Delay and area evaluation of regular SQRT CSLA: (a) group2,(b)group3, (c) group4, and (d) group5. F is a Full Adder.

III. RESULTS

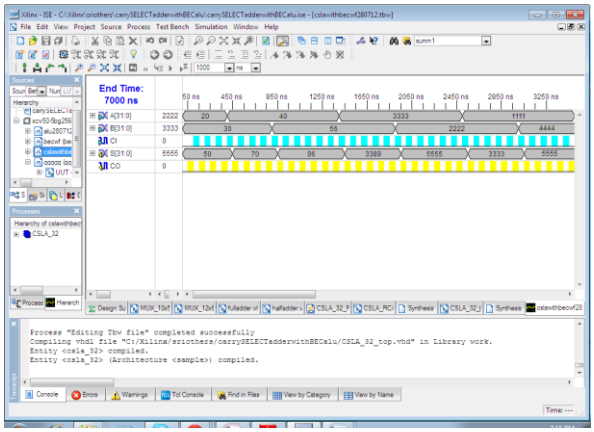
The proposed model is simulated in Xilinx using verilog language. A comparative analysis of CSLA Adders with RCA and BEC in terms of timing (delay)and power by using the device xcv50-5-bg256 is given in the table 2.



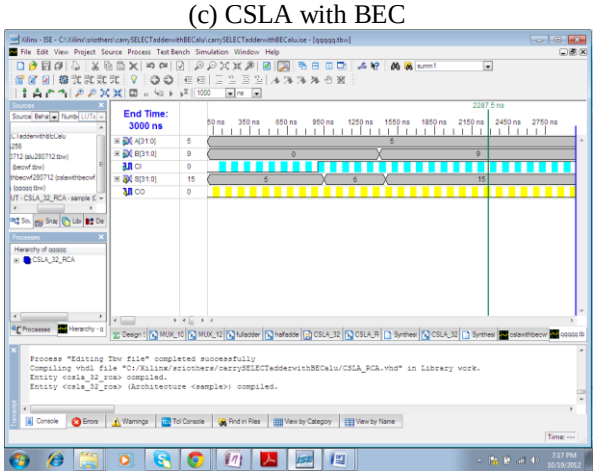
(a)



(b)



(c) CSLA with BEC



(d) CSLA with RCA

Fig.6: CSLA with BEC and RCA

The design output waveforms are given in the Fig.6(a) through (d).

IV. CONCLUSION

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic logic unit, the adder structures become a very critical hardware unit. In any book on computer arithmetic, someone looks that there exists a large number of different circuit architectures with different performance characteristics and widely used in the practice. Although many researches dealing with the adder structures have been done, the studies based on their comparative performance analysis are only a few. Digital Adders are the core block of DSP processors. The final carry propagation adder (CPA) structure of many adders constitutes high carry propagation delay and this delay reduces the overall performance of the DSPprocessor. In this project, qualitative evaluations of the CSLA adder with and without BEC architectures are given. Among the huge member of the adders we wrote VERILOG (Hardware Description Language) code for Carry skip and carry select adders to emphasize the common performance properties belong to their classes. With respect to delay time and power consumption we can conclude that the

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implementation of CSLA with BEC is efficient. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

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